[NAME OF DOCUMENT] Specification

[TITLE OF THE INVENTION]

Group-III Nitride Semiconductor Light-Emitting Diode and Electrode Therefor

[SCOPE OF CLAIM FOR PATENT]

[Claim 1] A group III-nitride semiconductor light-emitting diode comprising at least a first-conduction type single crystal substrate provided with a first-conduction type back-surface ohmic electrode on the back surface thereof, a buffer layer composed of a boron phosphide (BP) base material and formed on the surface of said single crystal substrate, a gallium nitride (GaN) related group III nitride crystal layer containing a light-emitting portion of hetero-junction structure and provided on said buffer layer, and a window layer composed of a conductive transparent oxide crystal layer and provided on said group-III nitride crystal layer, wherein a second-conduction type surface ohmic electrode conductive with said window layer is formed between the surface of said group-III nitride crystal layer and said window layer to come into contact with the surface of said group-III nitride crystal layer, and a pad electrode for wire bonding is formed in the center on the upper surface of said window layer.

[Claim 2] The group-III nitride semiconductor light-emitting diode as claimed in claim 1, wherein said

surface ohmic electrode is disposed in the periphery of said pad electrode.

[Claim 3] The group-III nitride semiconductor light-emitting diode as claimed in claim 1 or 2, wherein said surface ohmic electrode is disposed at the bilaterally symmetric position with respect to the center of said pad electrode.

[Claim 4] The group-III nitride semiconductor light-emitting diode as claimed in claims 1 to 3, wherein said surface ohmic electrodes are disposed at isometric positions from the center of said pad electrode.

[Claim 5] The group-III nitride semiconductor light-emitting diode as claimed in claims 1 to 4, wherein said surface ohmic electrode is composed of a plurality of electrodes disposed at equal intervals.

[Claim 6] The group-III nitride semiconductor light-emitting diode as claimed in claims 1 to 5, wherein said surface ohmic electrode is disposed in the region (hereinafter referred to as an "open light-emitting region") other than the projective region of the pad electrode on the surface of said group-III nitride crystal layer.

[Claim 7] The group-III nitride semiconductor light-emitting diode as claimed in claim 6, wherein the sum of areas of said surface ohmic electrodes is from 5 to 30%

of the total area of the open light-emitting region.

[Claim 8] The group-III nitride semiconductor light-emitting diode as claimed in claims 1 to 7, wherein the group-III nitride crystal layer in contact with said surface ohmic electrode comprises gallium phosphide nitride ($GaN_{1-X}P_X$; $0<X<1$).

[Claim 9] An electrode for group-III nitride semiconductor light-emitting diodes, which is used for a group-III nitride semiconductor light-emitting diode comprising at least a gallium nitride (GaN) related group-III nitride crystal layer containing a light-emitting portion of hetero-junction structure, and a window layer comprising a conductive transparent oxide crystal layer provided on said group-III nitride crystal layer, wherein a surface ohmic electrode conductive with said window layer is formed between the surface of said group-III nitride crystal layer and said window layer to come into contact with the surface of said group-III nitride crystal layer, and a pad electrode for wire bonding is formed in the center on the upper surface of said window layer.

[Claim 10] The electrode for group-III nitride semiconductor light-emitting diodes as claimed in claim 9, wherein said surface ohmic electrode is disposed in the periphery of said pad electrode.

[Claim 11] The electrode for group-III nitride

semiconductor light-emitting diodes as claimed in claim 9 or 10, wherein said surface ohmic electrode is disposed at the bilaterally symmetric position with respect to the center of said pad electrode.

[Claim 12] The electrode for group-III nitride semiconductor light-emitting diodes as claimed in claims 9 to 11, wherein said surface ohmic electrodes are disposed at isometric positions from the center of said pad electrode.

[Claim 13] The electrode for group-III nitride semiconductor light-emitting diodes as claimed in claims 9 to 12, wherein said surface ohmic electrode is composed of a plurality of electrodes disposed at equal intervals.

[Claim 14] The electrode for group-III nitride semiconductor light-emitting diodes as claimed in claims 9 to 13, wherein said surface ohmic electrode is disposed in the region (hereinafter referred to as an "open light-emitting region") other than the projective region of the pad electrode on the surface of said group-III nitride crystal layer.

[Claim 15] The electrode for group-III nitride semiconductor light-emitting diodes as claimed in claim 14, wherein the sum of areas of said surface ohmic electrodes is from 5 to 30% of the total area of the open light-emitting region.

[Claim 16] The electrode for group-III nitride semiconductor light-emitting diodes as claimed in claims 9 to 15, wherein the group-III nitride crystal layer in contact with said surface ohmic electrode comprises gallium phosphide nitride ($GaN_{1-X}P_X$; $0<X<1$).

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[Technical Field to Which the Invention Belongs]

The present invention relates to a group-III nitride semiconductor light-emitting diode (LED) having a configuration of ohmic electrodes suitable for diffusing a driving current of device over a wide range of the light-emitting region and also relates to an electrode for group-III nitride semiconductor light-emitting diodes.

[0002]

[Background Art]

A group-III nitride semiconductor light-emitting diode is fabricated by providing an electrode on a stacked layer structure having a pn-junction type light-emitting portion comprising, for example, aluminum gallium indium nitride ($Al_XGa_YIn_{1-X-Y}N$, where $0 \leqq X,Y \leqq 1$). In the stacked layer structure, a buffer layer is generally provided for relaxing lattice mismatch between the substrate material and the group-III nitride semiconductor layer constituting the stacked layer structure and thereby growing a high-

quality group-III nitride semiconductor layer (see, JP-A-2-229476 (the term "JP-A" as used herein means an "unexamined published Japanese patent application")). In the stacked layer structure for use in a light-emitting device using a sapphire (α-Al_2O_3 single crystal) substrate, the buffer layer is exclusively composed of aluminum gallium nitride (compositional formula; $Al_\alpha Ga_\beta N$, where $0 \leqq \alpha, \beta \leqq 1$) (see, JP-A-2-229476 *supra*).

In the case of a stacked layer structure using an insulating material such as sapphire for the substrate, an electrode for supplying a device driving current to LED comprising such a stacked layer structure, namely, an ohmic electrode, is disposed on p-type and n-type conductive layers constituting the stacked layer structure (see, JP-A-6-260682).

[0003]

Fig. 1 is a view schematically showing the cross-sectional structure of a conventional group-III nitride semiconductor LED 100 having a light-emitting portion 10 of pn-junction type double hetero (DH) structure comprising a sapphire substrate 101 having provided thereon, through a $Al_\alpha Ga_\beta N$ buffer layer 102 (where $0 \leqq \alpha, \beta \leqq 1$ and $\alpha+\beta=1$), a lower clad layer 103 composed of an n-type gallium nitride (GaN), a light-emitting layer 104 composed of gallium indium nitride ($Ga_Z In_{1-Y} N$, where $0 \leqq Y \leqq 1$), and an upper clad layer

105 composed of p-type GaN. The substrate 101 is insulating and therefore, p-type and n-type ohmic electrodes 106 and 107 must be provided on the surfaces of p-type conductive layer (p-type clad layer 105) and n-type conductive layer (n-type clad layer 103), respectively, constituting the stacked layer structure. The electrode 107 is formed through a cumbersome processing of cutting a part of the light-emitting portion 10. Furthermore, since a part of the light-emitting portion 10 is removed, the surface area of the light-emitting portion 10 decreases and a group-III nitride semiconductor LED ensuring high light emission intensity cannot be provided.

[0004]

In another known example, a stacked layer structure for use in a group-III nitride semiconductor blue LED is constructed using a conductive crystal such as gallium phosphide (GaP) or silicon, for the substrate (see, JP-A-2-275682). Also, a technique of forming a buffer layer from a boron phosphide (BP) base material in constructing this stacked layer structure is disclosed (see, JP-A-2-275682 *supra*). In the case of a stacked layer structure using a conductive crystal substrate, it is commonly performed to provide an electrode having first conduction type corresponding to the conductivity of the substrate crystal on the back surface of the substrate and dispose an

electrode having second conduction type opposed thereto on a stacked structure-constituting layer having conductivity opposite the conduction of the substrate crystal (see, JP-A-10-247761). In this conventional example of the electrode configuration, the light-emitting portion provided on the substrate surface needs not be eliminated and accordingly, the surface area of the light-emitting portion is not reduced. This is by itself advantageous in obtaining a high-intensity group-III nitride semiconductor LED.

[0005]

Fig. 2 is a view schematically showing a planary structure of a conventional group-III nitride semiconductor LED 200 comprising a first-conduction type ohmic electrode (back-surface ohmic electrode) on the back surface of a conductive substrate, and a second-conduction type ohmic electrode (surface ohmic electrode) on the surface of the stacked layer structure. The surface ohmic electrode 201 usually serves also as an electrode for wire-bonding (pad electrode) and is disposed only in the center part of one constituent layer 202 of the stacked layer structure (see, JP-A-2-275682). In still another conventionally known example, a surface ohmic electrode is attached with a band shape electrode directly contacting with the pad electrode in the center part (see, JP-A-11-168240).

[0006]

The surface ohmic electrode has been heretofore usually provided on an aluminum gallium nitride (Al_XGa_YN, where $0 \leqq X,Y \leqq 1$ and $X+Y=1$) crystal layer (see, JP-A-6-314822). However, aluminum nitride (AlN) and gallium nitride (GaN) are greatly small in the mobility as compared with other group III-V compound semiconductors such as gallium arsenide (GaAs) and indium phosphide (InP) (see, Yasuharu Suematsu, Hikari Device (Photo-Device), 1st ed., 8 imp., pp. 28-29, Corona Sya (May 15, 1997)). For example, the hole mobility of aluminum nitride (AlN) at room temperature is 14 $cm^2/V \cdot s$ and this is as low as about 1/30 in comparison, for example, with 500 $cm^2/V \cdot s$ of indirect transition-type boron phosphide (BP), (see, Photo-Device *supra*, pp. 28-29). Accordingly, by the conventional electrode configuration means of providing an ohmic electrode only on a constituent layer, a device operating current cannot be satisfactorily diffused over a wide range of the light-emitting portion and this is disadvantageous in obtaining a high-intensity group-III nitride semiconductor LED.

[0007]

With respect to the current diffusivity, by taking account of the fact that the physical properties of the group-III nitride semiconductor are inferior to other group

III-V compound semiconductors, a technique of using, as an ohmic electrode, a transparent metal thin film electrode directly connected to a pad electrode is disclosed (see, JP-A-6-314822). For example, a transparent ohmic electrode composed of gold (Au) thin film is provided almost whole of the surface of the gallium nitride (GaN) related group-III nitride semiconductor layer which is doped with p-type impurity (see, JP-A-6-314822 *supra*). However, in this conventional technique, the light emitted from the light-emitting portion is absorbed by the metal thin film constituting the electrode, as a result, the light emission which can be taken out outside the LED is disadvantageously reduced in the intensity.

[0008]

An indium·tin composite oxide (ITO) film has a high transmittance to blue light, green light or longer wavelength light emitted from a group-III nitride semiconductor LED (see, Tomei Doden Maku no Gijutsu (Transparent Conductive Film Technology), 1st ed., 1st imp., pp. 97-101, Ohmu Sya (March 30, 1999)). For more efficiently taking out the emitted light to the outside by utilizing this transmittance, a technique of providing a ITO transparent conductive film as a contact layer (a window layer for transmitting the emitted light) of the gallium nitride (GaN) layer and thereby fabricating a

group-III nitride semiconductor LED is known (see, (1) JP-A-49-122294, (2) JP-U-A-6-38265 (the term "JP-U-A" as used herein means an "unexamined published Japanese utility model application) and (3) Appl. Phys. Lett., Vol. 74, No. 26, pp. 3930-3932 (1999)).

[0009]

In many conventional techniques, a transparent conductive film of ITO or the like is disposed on a p-type GaN layer which is poor in the current diffusivity particularly due to difficulties in obtaining high hole concentration and mobility (see, JP-U-A-6-38265 and Appl. Phys. Lett., *supra*). However, the ITO cannot exhibit good ohmic contact with the group-III nitride semiconductor crystal layer and in the above-described case, the forward voltage (Vf) disadvantageously elevates (see, for more detail, Appl. Phys. Lett. *supra*, Vol. 74 (1999)).

[0010]

[Problems to be Solved by the Invention]

The present invention has been made by taking account of those problems in conventional techniques and proposes means for the configuration of ohmic electrodes for a group-III nitride semiconductor LED having a transparent conductive film of ITO or the like as the window layer for efficiently taking out the emitted light to the outside, which can allow the device operating current to diffuse

over a wide range of the light-emitting portion and high-intensity light emission to be taken out outside. Thus, the object of the present invention is to provide a high intensity group-III nitride semiconductor light-emitting diode having an ohmic electrode disposed by the above-described configuration means, and an electrode for the group-III nitride semiconductor light-emitting diode.

[0011]

In particular, the present invention is characterized in that a surface ohmic electrode is disposed on the surface of one constituent layer of a stacked layer structure at a suitable position with respect to the pad electrode, so that the device operating current can diffuse over a wide range of the light-emitting portion.

[0012]

[Means to Solve the Problems]

The present invention provides

(1) a group III-nitride semiconductor light-emitting diode comprising at least a first-conduction type single crystal substrate provided with a first-conduction type back-surface ohmic electrode on the back surface thereof, a buffer layer composed of a boron phosphide (BP) base material and formed on the surface of the single crystal substrate, a gallium nitride (GaN) related group III nitride crystal layer containing a light-emitting

portion of hetero-junction structure and provided on the buffer layer, and a window layer composed of a conductive transparent oxide crystal layer and provided on the group-III nitride crystal layer, wherein a second-conduction type surface ohmic electrode conductive with the window layer is formed between the surface of the group-III nitride crystal layer and the window layer to come into contact with the surface of the group-III nitride crystal layer, and a pad electrode for wire bonding is formed in the center on the upper surface of the window layer.

[0013]

Also, the present invention provides

(2) the group-III nitride semiconductor light-emitting diode as described in (1), wherein the surface ohmic electrode is disposed in the periphery of the pad electrode;

(3) the group-III nitride semiconductor light-emitting diode as described in (1) or (2), wherein the surface ohmic electrode is disposed at the bilaterally symmetric position with respect to the center of the pad electrode;

(4) the group-III nitride semiconductor light-emitting diode as described in (1) to (3), wherein the surface ohmic electrodes are disposed at isometric positions from the center of the pad electrode;

(5) the group-III nitride semiconductor light-emitting diode as described in (1) to (4), wherein the surface ohmic electrode is composed of a plurality of electrodes disposed at equal intervals;

(6) The group-III nitride semiconductor light-emitting diode as described in (1) to (5), wherein the surface ohmic electrode is disposed in the region (hereinafter referred to as an "open light-emitting region") other than the projective region of the pad electrode on the surface of the group-III nitride crystal layer;

(7) the group-III nitride semiconductor light-emitting diode as described in (6), wherein the sum of areas of the surface ohmic electrodes is from 5 to 30% of the total area of the open light-emitting region; and

(8) the group-III nitride semiconductor light-emitting diode as described in (1) to (7), wherein the group-III nitride crystal layer in contact with the surface ohmic electrode comprises gallium phosphide nitride ($GaN_{1-X}P_X$; $0<X<1$).

[0014]

Also, the present invention provides

(9) an electrode for group-III nitride semiconductor light-emitting diodes, which is used for a group-III nitride semiconductor light-emitting diode comprising at least a gallium nitride (GaN) related group-

III nitride crystal layer containing a light-emitting portion of hetero-junction structure, and a window layer comprising a conductive transparent oxide crystal layer provided on the group-III nitride crystal layer, wherein a surface ohmic electrode conductive with the window layer is formed between the surface of the group-III nitride crystal layer and the window layer to come into contact with the surface of the group-III nitride crystal layer, and a pad electrode for wire bonding is formed in the center on the upper surface of the window layer.

[0015]

Also, the present invention provides

(10) the electrode for group-III nitride semiconductor light-emitting diodes as described in (9), wherein the surface ohmic electrode is disposed in the periphery of the pad electrode;

(11) the electrode for group-III nitride semiconductor light-emitting diodes as described in (9) or (10), wherein the surface ohmic electrode is disposed at the bilaterally symmetric position with respect to the center of the pad electrode;

(12) the electrode for group-III nitride semiconductor light-emitting diodes as described in (9) to (11), wherein the surface ohmic electrodes are disposed at isometric positions from the center of the pad electrode;

(13) the electrode for group-III nitride semiconductor light-emitting diodes as described in (9) to (12), wherein the surface ohmic electrode is composed of a plurality of electrodes disposed at equal intervals;

(14) the electrode for group-III nitride semiconductor light-emitting diodes as described in (9) to (13), wherein the surface ohmic electrode is disposed in the region (hereinafter referred to as an "open light-emitting region") other than the projective region of the pad electrode on the surface of the group-III nitride crystal layer;

(15) the electrode for group-III nitride semiconductor light-emitting diodes as described in (14), wherein the sum of areas of the surface ohmic electrodes is from 5 to 30% of the total area of the open light-emitting region; and

(16) the electrode for group-III nitride semiconductor light-emitting diodes as described in (9) to (15), wherein the group-III nitride crystal layer in contact with the surface ohmic electrode comprises gallium phosphide nitride ($GaN_{1-X}P_X$; $0<X<1$).

[0016]

[Mode for Carrying Out the Invention]

Fig. 3 is a schematic sectional view for explaining the group-III nitride semiconductor LED 300 or the

electrode construction thereof according to the first embodiment of the invention described in (1) or (9) above. In the LED 300 according to the first embodiment, the matrix material is a stacked layer structure 31 where a single crystal having conductivity is used as the substrate 301. By using this conductive single crystal as the substrate, a first-conduction type ohmic electrode can be provided on the back surface of the substrate as the back-surface ohmic electrode 309. More specifically, unlike conventional group-III nitride LEDs using a substrate of electrical insulating single crystal such as sapphire, the ohmic electrode is provided without involving any partial removal of the light-emitting portion and therefore, the light-emitting portion is evaded from the reduction in the surface area, which is advantageous in obtaining a group-III nitride LED having high light emission intensity. Furthermore, when a single crystal having conductivity and also having cleavage property is used as the substrate, the separation into individual devices can be readily and simply performed utilizing the cleavage of the crystal and thereby, a group-III nitride LED can be extremely readily fabricated. Examples of the single crystal having both conductivity and cleavage property, which can be suitably used as the substrate, include silicon (Si), gallium phosphide (GaP) and gallium arsenide (GaAs). In stacking a

group-III nitride semiconductor layer on the surface of a substrate, the deposit is generally performed at a high temperature in excess of about 800°C and on considering this, silicon single crystal (silicon) and the like having heat resistance at high temperatures are suitably used as the substrate. For example, a p-type or a n-type silicon having a plane azimuth of {100} or {111} is suitable as the substrate.

[0017]

On the surface of the substrate 301 comprising a conductive crystal, a buffer layer 302 composed of a boron phosphide (BP) base material is provided. The boron phosphide (BP) base material means a group III-V compound semiconductor containing at least boron (B) and phosphorus (P) as constituent elements. Examples of the BP material include boron nitride phosphide ($BN_{1-X}P_X$, where $0<X<1$) and boron gallium phosphide ($B_{1-Y}Ga_YP$, where $0<Y<1$), in addition to boron phosphide (BP). The BP material is reduced in the lattice mismatch with a group-III nitride semiconductor constituting the pn-junction type double hetero (DH) junction light-emitting portion 30, such as gallium nitride (GaN). For example, $BN_{0.03}P_{0.97}$ (lattice constant: 4.510 Å) having a nitrogen composition ratio (=1-X) of 0.03 (3%) is advantageous in that a buffer layer capable of lattice-matching with cubic crystal GaN can be formed therefrom. By

virtue of this good lattice matching, the buffer layer comprising a BP material exerts an effect of giving an upper layer reduced in the density of crystal defects such as misfit dislocation, and having excellent crystallinity.
[0018]

The BP-based buffer layer mainly composed of an amorphous body in the as-grown state is particularly effective in relaxing the lattice mismatch between the conductive single crystal material constituting the substrate and the constituent layer of the stacked layer structure. This is because the crystal layer mainly composed of an amorphous body is crystallized while absorbing the lattice distortion originated from the lattice mismatch accompanying the film formation of the upper layer and therefore, exerts an effect of giving a good quality upper layer. The BP-based buffer layer mainly composed of an amorphous body can be obtained, for example, by performing the film formation at a temperature in excess of about 200°C but up to 500°C using a triethylboron ($(C_2H_5)_3B$)/phosphine (PH_3) reaction-system metal organic chemical vapor deposition (MOCVD) method, similarly to other constituent layers of the stacked layer structure or by performing the film formation at a film formation temperature of about 150 to about 750°C using a boron trichloride (BCl_3)/phosphorus trichloride (PCl_3) reaction-

system halogen vapor phase epitaxy (VPE) method. The film formation temperature is preferably from about 200 to about 500°C (see, JP-A-2000-58451). Irrespective of the vapor phase growth means, the most important condition for obtaining a BP-based buffer layer mainly composed of an amorphous body is the film formation temperature. If the film formation temperature is less than about 200°C, the thermal decomposition of starting materials does not satisfactorily proceed and therefore, stable formation of the buffer layer cannot be attained, whereas if the growth temperature exceeds 500°C, a polycrystalline layer is readily formed and this is disadvantageous because on the polycrystalline layer comprising randomly gathered single crystals, crystals readily grow in random azimuths by reflecting the orientation (coordinate direction) of each single crystal constituting the polycrystalline layer and the upper layer obtained disadvantageously fails in having a flat surface. The difference in main constituent elements of the buffer layer can be known by general analysis means such as X-ray diffraction analysis or electron-beam diffraction.

[0019]

The buffer layer may also be composed of a low-temperature buffer layer comprising a BP material and a single crystal layer comprising a BP material, where the

low-temperature buffer layer is formed at a relatively low temperature of 200 to 500°C and the single crystal layer is formed on the low-temperature buffer layer at a temperature higher than the film formation temperature of the low-temperature buffer layer. The BP-based crystal layer formed through the low-temperature buffer layer works out to a single crystal layer reduced in the density of crystal defects and having excellent crystallinity and this single crystal layer is effective in obtaining an upper layer reduced in the defect density. In other words, the buffer layer composed of a plurality of layers of a BP-based low-temperature buffer layer and a BP-based high-temperature single crystal layer formed on the low-temperature buffer layer, is effective in obtaining an upper layer having excellent crystallinity. Examples of the buffer layer structure coming under this category include a stratified buffer layer composed of two layers of a low-temperature buffer layer comprising amorphous boron phosphide (BP) and a BP single crystal layer. The high-temperature buffer layer is preferably formed at a film formation temperature of approximately from 800 to 1,200°C using vapor phase growth means such as MOCVD method described above.

[0020]

On the low-temperature buffer layer or on the stratified buffer layer, a light-emitting portion is

constructed. The light-emitting portion is a portion undertaking the light emission and is composed of at least a light-emitting layer and a clad layer. The light-emitting portion can be composed of either a single hetero structure or a double hetero junction structure. The light-emitting portion is preferably composed of a double hetero (DH) junction structure, so that high-intensity light emission can be obtained due to the carrier "confinement effect" as compared with the case having a single hetero junction structure. Fig. 3 shows a light-emitting portion 30 of pn-junction DH structure composed of a light-emitting layer 304 sandwiched by a lower clad layer 303 and an upper clad layer 305 according to the first embodiment. The intensity of light emitted from the light-emitting portion depends on the crystallinity of a functional layer constituting the light-emitting portion, particularly a crystal layer as the light-emitting layer. In general, as the crystal layer used has higher quality reduced in dislocation or defect, the light emission obtained can have higher intensity. Accordingly, the light-emitting portion is preferably composed of a crystal layer reduced in the lattice mismatch with the above-described low-temperature buffer layer or stratified buffer layer. For example, cubic boron gallium phosphide ($B_{0.97}Ga_{0.03}P$) having a gallium (Ga) composition ratio of 0.03 (3%), a cubic gallium nitride phosphide

($GaN_{0.97}P_{0.03}$) having a phosphorus composition ratio of 0.03 and a cubic gallium indium nitride ($Ga_{0.88}In_{0.12}N$) having an indium composition ratio of 0.12 all have the same lattice constant of 4.566 Å. Therefore, on a $B_{0.97}Ga_{0.03}P$ buffer layer, a lattice-matched system light-emitting portion can be formed using a $GaN_{0.97}P_{0.03}$ clad layer and a $Ga_{0.88}In_{0.12}N$ light-emitting layer. That is, the light-emitting portion can be constructed from a high-quality crystal layer reduced in the density of crystal defects ascribable to the lattice mismatch.

[0021]

The electrode on the surface side of the group-III nitride semiconductor 300 is constructed by disposing surface ohmic electrodes 308 on the surface of one constituent layer of the stacked layer structure 31, for example, the upper clad layer 305 constituting the light-emitting portion 30 of pn-junction DH structure, superposing thereon a window layer 306 comprising a conductive transparent oxide crystal layer such as ITO, to cover the surfaces of the upper clad layer 305 and the surface ohmic electrode 308 and also to be conductive with the surface ohmic electrode 308, and providing a pad electrode 307 in the center part on the window layer 306. That is, as a characteristic feature, the surface ohmic electrodes 308 are disposed on the surface of one

constituent layer (the upper clad layer 305 in the LED 300 shown in Fig. 3) of a stacked layer structure 31 for use in a group-III nitride semiconductor LED 300, independently of the pad electrode 307 and at the same time while preventing their direct contact with the pad electrode 307. The pad electrode 307 and the surface ohmic electrode 308 are conductive through the conductive transparent oxide crystal layer such as ITO of the window layer 306. Other than ITO, the window layer 306 can also be similarly formed from a good conductor transparent material having a transmittance sufficiently high to allow the efficient ejection of emitted light to the outside and at the same time, having capability of supplying a device operating current to the surface ohmic electrode 308. Examples of the constituent material other than ITO include zinc oxide (ZnO) and a mixed oxide of zinc (Zn) and silicon (Si).

[0022]

In particular, the present invention is characterized in that surface ohmic electrodes 308 are planarly disposed in the periphery of a pad electrode 307 to fabricate a group-III nitride semiconductor LED. Fig. 4 shows a configuration example of surface ohmic electrodes 308 according to the first embodiment. The surface ohmic electrodes 308 disposed on the surface of one constituent layer 305 (see, Fig. 3) of the stacked structure 31 (see,

Fig. 3) at the bilaterally symmetric positions centered in the pad electrode 307 distribute and diffuse the device operating current into the inside of the one constituent layer 305 and in turn into the light-emitting portion 30 (see Fig. 3). In an example of the construction different from the case having a plurality of the surface ohmic electrodes 308 shown in Fig. 4, the surface ohmic electrode may be composed of a single cyclic metal electrode. Unlike the configuration means shown in conventional techniques (see, JP-A-57-111076) where ohmic electrodes are islanded in the intermediate region between pad electrodes provided not at the center of the light-emitting device but in the periphery of the device, in the present invention, the surface ohmic electrode is planarly disposed in the periphery of the pad electrode provided at the center of the light-emitting device.

[0023]

Describing by referring to Fig. 3, the light emission in the projective region 307a of the pad electrode 307, present beneath the pad electrode 307, cannot be efficiently taken out to the outside because the light emitted from the light-emitting portion 30 is shielded by the pad electrode. In other words, the device operating current supplied to the projective region 307a from the pad electrode 307 through the window layer 306 is wasted and

fails in effectively contributing to the improvement of the light emission intensity of the device.

Accordingly, in the second embodiment of the present invention, the surface ohmic electrodes 308 are disposed on the surface of the region 307b (hereinafter referred to as an "open light-emitting region 307b") other than the projective region 307a of the pad electrode 307 on the group-III nitride crystal layer constituting the stacked layer structure 31. Fig. 4 shows a schematic plan view of a group-III nitride semiconductor LED having surface ohmic electrodes of the present invention. The ohmic electrodes 308 disposed in the open light-emitting region 307b exert an effect of preferentially passing and diffusing the device operating current to the open light-emitting region 307b. When the device operating current is allowed to flow only to the open light-emitting region 307b which is opened to the outside and therefore, facilitated in taking out the emitted light to the outside, the current density of the device operating current which in turn flows to, for example, the light-emitting portion 30 having a gallium indium nitride ($Ga_YIn_{1-Y}N$, where $0 \leqq Y \leqq 1$) light-emitting layer 304, located below the open light-emitting region 307b, is increased and this is advantageous in obtaining a group-III nitride semiconductor LED having high-intensity light emission.

[0024]

In the third embodiment of the present invention, the surface ohmic electrode is disposed on the surface of the open light-emitting region at the bilaterally symmetric position with respect to the center of the pad electrode. The surface ohmic electrode disposed in the periphery of the pad electrode to have a positional relationship of bilateral symmetry exerts an effect of homogeneously diffusing the device operating current over a wide range of the light-emitting portion. In particular, when the surface ohmic electrode is disposed on the surface of the open light-emitting region and at the same time, in the bilaterally symmetric position with respect to the center of the pad electrode, the current density of the device operating current flowing to the open light-emitting region can be equalized and this is advantageous in obtaining a group-III nitride semiconductor LED having homogeneous (in-plane) emission intensity.

[0025]

In the forth embodiment of the present invention, the surface ohmic electrodes are provided in the isometric positions from the center of the pad electrode on the surface of the open light-emitting region. The ohmic electrodes provided in the periphery of the pad electrode at equal intervals exert an effect of uniformly diffusing

the device operating current over a wide range of the light-emitting portion. In particular, the surface ohmic electrodes regularly disposed on the surface of the open light-emitting region at the same distance from the pad electrode provides an effect of equalizing the current density of the device operating current flowing to the open light-emitting region and making homogeneous light emission intensity in the open light-emitting region. The surface ohmic electrode configuration according to the fourth embodiment can be constructed, for example, by disposing surface ohmic electrodes at a plurality of positions on the circumference of a concentric circle centered in the planar center of the pad electrode. The surface ohmic electrodes provided in several positions are not all necessary to have the same planar shape but at least the surface ohmic electrodes located in the bilaterally symmetric positions with respect to the pad electrode preferably have the same planar shape, so that the potential distribution can be made bilaterally symmetric in the open light-emitting region and thereby light emission having homogeneous intensity can be obtained from the open light-emitting region.

[0026]

In the fifth embodiment of the present invention, the surface ohmic electrode is composed of a plurality of

electrodes disposed at equal intervals on the surface of one constituent layer of the stacked structure. By disposing a plurality of surface ohmic electrodes at equal intervals in the peripheral region of the pad electrode on the surface of one constituent layer, the device operating current supplied through the window layer from the pad electrode can be allowed to uniformly flow to the light-emitting portion. In particular, when the surface ohmic electrodes are provided at constant intervals on the surface of the open light-emitting region while preventing these from coming into contact with the projective region of the pad electrode, the device operating current in a high and uniform current density can preferentially flow almost exclusively to the open light-emitting region, that is, the region other than the projective region of the pad electrode, where the emitted light can be easily taken out to the outside. This is advantageous in obtaining a group-III nitride semiconductor LED having homogeneous (in-plane) emission intensity. The surface ohmic electrodes provided at equal intervals are not always necessary to have the same planar shape but the surface ohmic electrodes disposed at symmetric positions with respect to the pad electrode preferably have the same planar shape.

[0027]

In particular, the surface ohmic electrodes disposed

exclusively in the open light-emitting region by utilizing all construction means according to the third to fifth embodiments above provide a greatest effect in allowing the device operating current to preferentially flow to the open light-emitting region in a homogeneous current density. Fig. 5 is a schematic plan view showing one configuration form of surface ohmic electrodes 508, where the contents described in the third to fifth embodiments are generally included. To speak specifically, this is a schematic plan view of a group-III nitride semiconductor LED having electrodes constructed such that surface ohmic electrodes 508 are disposed in the open light-emitting region 507b (a) at the bilaterally symmetric positions with respect to the pad electrode 507 in the peripheral region of the pad electrode 507 while not coming into contact with the projective region of the pad electrode 507, (b) at several portions on the circumferences 509 and 510 of two concentric circles of a radius d_1 or d_2 (provided that $d_1>d_2$) centered in the center of the pad electrode 507, which are located at the same distance from the center 507c of the pad electrode 507, and (c) at equal intervals from each other on the same circumference (509 or 510). By disposing, as shown in Fig. 5, the surface ohmic electrodes 508 so as to equalize the current density of the device operating current flowing to the open light-emitting region 507b, the

device operating current can preferentially and homogeneously flow to the open light-emitting region 507b and therefore, the group-III nitride semiconductor LED obtained can be free of extinction in the limb of LED and favored with excellent homogeneity of the (in-plane) emission intensity.

[0028]

If the area of the surface ohmic electrode contacting with the constituent layer of the stacked layer structure, on which the electrode is provided, can be reduced, the injection density (current density) of the device operating current may be increased and the light emission intensity may be elevated. However, if the contact area between the surface ohmic electrode and the constituent layer is reduced, the ohmic contact resistance increases to incur useless increase of the forward voltage (forward vias: Vf) and this is disadvantageous. Accordingly, in the sixth embodiment of the present invention, the ratio (=A/B) between the sum (=A) of areas of the surface ohmic electrodes and the total area (=B) of the open light-emitting region is specified to be from 5 to 30%. The term "total area (=B) of the open light-emitting region" as used herein means an area obtained by subtracting the bottom area of the pad electrode corresponding to the surface area in the projective region of the pad electrode from the

surface area of one constituent layer where surface ohmic electrodes are disposed. The term "sum (=A) of areas of the surface ohmic electrodes" as used herein means, in the case of a single ohmic electrode, the planar area of the ohmic electrode and in the case of a plurality of ohmic electrodes, the sum of planar areas of respective ohmic electrodes.

[0029]

If the ratio of the sum (=A) of areas of surface ohmic electrodes occupying in the total area (=B) of the open light-emitting region is less than 5%, the current density of the device operating current increases to bring about improvement on the light emission intensity, however, abrupt increase in the Vf disadvantageously occurs when the forward voltage is set to 20 mA. For example, as compared with the group-III nitride semiconductor LED having a ratio within the above-described preferred range, the Vf increases by about 20 to 30% and sometimes elevates in excess of 4.5 V. As the area of the surface ohmic electrode occupying in the open light-emitting region increases, the Vf decreases. However, the surface ohmic electrode is usually composed of a metal which absorbs the light emitted from the light-emitting portion and therefore, as the ratio (=A/B) elevates, the degree of absorption of the emitted light by the surface ohmic electrode comprising the metal

increases, as a result, the light emission intensity disadvantageously undergoes great decrease. If the ratio between the sum (=A) of areas of the surface ohmic electrodes and the total area (=B) of the open light-emitting region exceeds 30%, the light emission intensity of LED, for example, at a forward current of 20 mA may decrease to about 40 to 50%, as compared with a group-III nitride semiconductor LED having a ratio within the above-described preferred range.

[0030]

For example, in the case of an LED where a circular pad electrode having a diameter of 120 μm is mounted and the surface of LED is in the form of a square having a one-side length of 350 μm, the total area of the open light-emitting region obtained by subtracting the projective region of the pad electrode from the planar surface area of LED is about 1.1×10^{-3} cm^2. With this total area (=B) of the open light-emitting region, when the sum (=A) of areas of the surface ohmic electrodes is adjusted to from 5.5×10^{-5} cm^2 (A/B=0.05) to 3.3×10^{-4} cm^2 (A/B=0.30), the group-III nitride semiconductor LED fabricated can have high light emission intensity and at the same time, low forward voltage. Furthermore, for example, when 12 pieces in total of circular surface ohmic electrodes having a diameter of 20 μm are disposed in the open light-emitting region having a

total area of about 1.1×10^{-3} cm^2 (=B), the sum (=A) of areas of the surface ohmic electrodes is 9.4×10^{-6} cm^2 and a group-III nitride semiconductor LED having a ratio (A/B) of about 8.6% can be fabricated. This ratio (A/B) is usually adjusted by appropriately designing the diameter, width or length of the surface ohmic electrode. In particular, when the ratio is adjusted to from about 7% to about 10%, the fabricated group-III nitride semiconductor LED can advantageously maintain high light emission intensity and low Vf. In the case of providing the surface ohmic electrode on the surface of p-type group-III nitride semiconductor layer, the ratio (=A/B) is preferably set larger than in the case of disposing the surface ohmic electrode on the surface of n-type group-III nitride semiconductor layer, so as to equalize the current density of the device operating current flowing to the open light-emitting region. This is because as compared with the n-type group-III nitride semiconductor, the p-type group-III nitride semiconductor is small in the carrier mobility and narrow in the range where the device operating current can diffuse and therefore, the contact area of the surface ohmic electrode with the semiconductor layer must be enlarged to broaden the range where the current diffuses. Particularly, in the case of a p side-up type LED where the surface ohmic electrode is provided on the surface of a p-

type group-III nitride semiconductor layer, the ratio (A/B) is preferably set to about 10% larger than the ratio (A/B) recognized suitable in the case of an n side-up type LED and by setting as such, good results can be obtained.

[0031]

The useless increase of the forward voltage, which is dependent on the construction material of one constituent layer (contact layer) where the surface ohmic electrode is provided, can be inhibited by reducing the contact resistance of the surface ohmic electrode. Accordingly, in the seventh embodiment of the present invention, the constituent layer of the stacked layer structure, where the surface ohmic electrode is disposed, is composed of a gallium nitride phosphide ($GaN_{1-X}P_X$, where $0<X<1$) crystal layer. Conventionally, gallium nitride (GaN) has been used for the contact layer in many cases (see, JP-A-6-268259). However, when $GaN_{1-X}P_X$ ($0<X<1$) is used, the band gap can be varied by adjusting the phosphorus composition ratio (=X) (see, Appl. Phys. Lett., Vol. 60, No. 20, pp. 2520-2542 (1992)). In other wards, depending on the phosphorus composition ratio (=X), the contact layer can be formed from a group-III nitride semiconductor material having a smaller band gap than gallium nitride (GaN) and therefore, a surface ohmic electrode having a small contact resistance can be advantageously formed.

[0032]

For example, the transition energy corresponding to the blue light emission at a wavelength of 450 nm (nanometer) is about 2.75 eV and the transition energy corresponding to the green light emission at a wavelength of 520 nm is about 2.38 eV. Accordingly, when $GaN_{1-X}P_X$ ($0<X<1$) used for the contact layer has a band gap of about 2.8 eV or more in the case of LED having a light-emitting layer of giving blue light emission or a band gap of about 2.4 eV or more in the case of LED having a light-emitting layer of giving green light emission, the contact layer constructed can be inhibited from absorbing the emitted light. In view of the non-liner change of gallium nitride phosphide ($GaN_{1-X}P_X$, where $0<X<1$) (see, Appl. Phys. Lett., Vol. 60, *supra*), a contact layer having excellent transmission for the blue or green light emission can be composed of $GaN_{1-X}P_X$ ($0<X \leqq 0.05$) having a phosphorus composition ratio (=X) of 5% (X=0.05) or less. The $GaN_{1-X}P_X$ ($0<X\leqq0.05$) having a phosphorus composition ratio (=X) of 5% (X=0.05) or less has a band gap in excess of 2.8 eV at room temperature and to be advantageous, this can also be used as a clad layer for sandwiching a light-emitting layer which brings about blue or green light emission or as a contact layer serving also as the clad layer. The surface ohmic electrode provided on the surface of the contact

layer comprising $GaN_{1-x}P_x$ can be composed of, in the case of n-type contact layer, gold (Au) or a gold alloy such as gold·germanium (Au·Ge) and gold·tin (Au·Sn), and in the case of p-type contact layer, the surface ohmic electrode can be composed of a zinc (Zn)-containing alloy such as indium·zinc (In·Zn) and gold·zinc (Au·Sn), or a gold·beryllium (Au·Be) alloy.

[0033]

[Mode of Operation]

The surface ohmic electrode disposed in the periphery of the pad electrode on the surface of the group-III nitride semiconductor crystal layer of the present invention can provide an effect of allowing the device operating current supplied through a window layer from the pad electrode on the window layer to diffuse over a wide range of the light-emitting layer.

[0034]

The surface ohmic electrode disposed in the region (open light-emitting region) other than the projective region of the pad electrode on the surface of the group-III nitride semiconductor crystal layer can provide an effect of allowing the device operating current to preferentially flow to the open light-emitting region where the emitted light can be easily taken out to the outside.

[0035]

The surface ohmic electrode disposed on the surface of the open light-emitting region at the bilaterally symmetric position with respect to the center of the pad electrode can provide an effect of allowing the device operating current to preferentially and uniformly diffuse in the open light-emitting region.

[0036]

The surface ohmic electrodes disposed on the surface of the open light-emitting region at isometric positions from the center of the pad electrode can provide an effect of allowing the device operating current to more uniformly flow to the open light-emitting region.

[0037]

The surface ohmic electrode composed of a plurality of electrodes disposed at equal intervals from each other can provide an effect of equalizing the current density of the device operating current flowing to the open light-emitting region.

[0038]

The surface ohmic electrodes controlled such that the sum of their areas is from 5 to 30% of the total area of the open light-emitting region can provide an effect of elevating the light emission intensity without causing useless increase of the forward voltage.

[0039]

The gallium nitride phosphide ($GaN_{1-x}P_x$, where $0<X<1$) crystal layer used for the contact layer of the surface ohmic electrode can provide an effect of giving a surface ohmic electrode having small contact resistance.

[0040]

[Examples]

(Example 1)

The group-III nitride semiconductor LED according to the present invention is described in greater detail below by referring to the Examples. Fig. 6 is a schematic plan view of a group-III nitride semiconductor LED 600 of Example 1. Fig. 7 is a schematic sectional view cut along the broken line A-A' of LED 600 shown in Fig. 6.

[0041]

LED 600 was fabricated based on a stacked layer structure 61 comprising a substrate 601 having provided thereon the following layers 602 to 605:

(1) a substrate 601 composed of a boron (B)-doped Si single crystal having a p-type conductive (100) face,

(2) a low-temperature buffer layer 602 comprising a Zn-doped p-type boron phosphide (BP) and having a layer thickness of about 20 nanometer (nm), which was grown at 350°C by a normal pressure (atmospheric pressure) MOCVD method in a reaction system of triethylborane

$((C_2H_5)_3B)$/phosphine (PH_3)/hydrogen (H_2) while setting the feed ratio (V/III ratio) between PH_3 and $(C_2H_5)_3B$ to about 300,

(3) a Zn-doped p-type boron phosphide (BP) single crystal layer 603 having a layer thickness of about 0.8 μm and a carrier concentration of about 1×10^{18} cm^{-3}, which was stacked on the p-type BP low-temperature buffer layer 602 at about 1,000°C by an atmospheric pressure MOCVD method in a reaction system of trimethyl gallium ($(CH_3)_3Ga$)/ammonia (NH_3)/PH_3/H_2 using dimethylzinc ($(CH_3)_2Zn$) as a starting material for the Zn doping,

(4) a light-emitting layer 604 comprising an n-type gallium indium nitride mixed crystal ($Ga_{0.94}In_{0.06}N$) and having a layer thickness of about 8 nm, which was grown at 880°C by an atmospheric pressure MOCVD method in a reaction system of $(CH_3)_3Ga$/trimethyl indium ($(CH_3)_3In$)/NH_3/H_2 to have a multi-phase structure consisting of a plurality of phases different in the indium composition with the average indium (In) composition ratio being about 0.06 (6%), and

(5) an n-type gallium nitride (GaN) layer 605 having a layer thickness of about 0.1 μm and a carrier concentration of about 2×10^{18} cm^{-3}, which was grown at 1,080°C by an atmospheric pressure MOCVD method in a reaction system of $(CH_3)_3Ga/NH_3/H_2$.

[0042]

The light-emitting portion 60 having a pn junction-type double hetero (DH) junction structure was constructed using the p-type BP single crystal layer 603 stacked on the low-temperature buffer layer 602 as a lower clad layer, the $Ga_{0.94}In_{0.06}N$ layer 604 as a light-emitting layer and the n-type GaN layer 605 as a upper clad layer. In the open light-emitting region 607b other than the projective region 607a of the pad electrode 607 on the surface of the upper clad layer 605, n-type surface ohmic electrodes 609 comprising gold (Au) were distributed and disposed. The n-type surface ohmic electrodes 609 were formed by a method of once covering the entire surface of the upper clad layer 605 with a gold (Au) film by vacuum evaporation and then allowing the Au evaporation film to remain only in the desired regions through patterning using a known photolithography technique. The Au evaporation film adhering to the region other than the desired regions was removed by a wet etching solution. Thereafter, on the surface of the upper clad layer 605 while allowing the n-type surface ohmic electrodes 609 to remain thereon, a window layer 606 comprising an indium·tin composite oxide (ITO) was deposited by an ordinary high-frequency spattering method. The ITO film constituting the window layer 606 had a resistivity of about 6×10^{-4} Ωcm and a layer

thickness of about 550 nanometer (nm).

[0043]

In addition to the surface ohmic electrodes 609, the following electrodes were formed on the stacked layer structure 61 using a known photolithography technique or the like, thereby fabricating the LED 600:

(1) a circular pad electrode 607 comprising gold (Au) and having a diameter of 120 μm, which was formed in the center part of the window layer 606, and

(2) a p-type back surface ohmic electrode 608 comprising aluminum (Al), which was formed almost throughout the back surface of the Si single crystal substrate 601.

[0044]

The n-type surface ohmic electrode 609 was composed of metal electrodes comprising Au and having a diameter of 30 μm and the same circular shape, which were disposed at 8 positions in total on the surface of the open light-emitting region 607b. The sum (=B) of areas of the n-type surface ohmic electrodes 609 was about 5.6×10^{-5} cm^2. The surface ohmic electrodes 609 were distributed and disposed at the positions on a circular circumference having a radius of 120 μm and centered in the center of the pad electrode 607 while taking a center angle of 45°C to lie apart from each other at equal intervals of about 46 μm in

terms of the rectilinear distance.

Thereafter, the stacked layer structure 60 having formed thereon electrodes 607 to 609 was divided into individual chips 600 by general scribing means utilizing the cleavage property in the [110] direction of the Si single crystal substrate 601. The planar shape of the chip 600 was a square having a one-side length of about 350 μm, the diameter of the pad electrode 607 was 120 μm as described above and the area (=A) of the open light-emitting region 607b was about 1.1×10^{-3} cm^2. Accordingly, the ratio (=A/B) of the sum of areas of the surface ohmic electrodes occupying in the total area of the open light-emitting region 607b was about 5.1%.

[0045]

An operating current was passed between the surface ohmic electrodes 609 and the back surface ohmic electrode 608 through the pad electrode 607 and the window layer 606, as a result, the following light emission properties were obtained.

(a) Light emission wavelength: 440 nm

(b) Light emission luminance: 1.6 candela (cd) (provided that forward current = 20 mA)

(c) Forward voltage: 3.8 Volt (V) (provided that forward current = 20 mA)

(d) Backward voltage: 20 V or more (provided that

reverse current = 10 μA)

By constructing the surface ohmic electrode as in this Example, the device operating current was advantageously allowed to preferentially flow to the open light-emitting region and therefore, a group-III nitride semiconductor light-emitting device having high emission intensity was provided.

[0046]

(Example 2)

In Example 2, the present invention is described by referring to the case where a group-III nitride semiconductor light-emitting diode 700 different in the configuration of surface ohmic electrodes 609 from Example 1 was manufactured using the same stacked layer structure 61 as the structure described in Example 1.

[0047]

Fig. 8 shows a schematic plan view of a group-III nitride semiconductor LED 700 according to Example 2. In Fig. 8, the same portions as those shown in Fig. 6 are indicated by the same reference numbers as in Fig. 6 and not described here.

[0048]

In the group-III nitride semiconductor LED 700 of Example 2, a frame-shaped surface ohmic electrode 609 having a stratified structure consisting of a gold (Au)

lower layer and a nickel oxide (NiO_x, where X is about 1) upper layer was provided on the open light-emitting region 607b in the periphery of the pad electrode 607. The outer circumference of the frame-shaped surface ohmic electrode 609 had a square form by reflecting the outer shape of the square LED 700 having a one-side length of 320 μm and the inner circumference had a circular shape analogous to the circular pad electrode 607 having a diameter of 120 μm. The distance from the center 607c of the pad electrode 607 to the outer circumference of the frame-shaped surface ohmic electrode 609 was 120 μm and the distance to the circular inner circumference was 100 μm in terms of the radius from the center 607c of the pad electrode 607. The surface ohmic electrode 609 having a planar shape as if it is resultant from punching out a circular region in a diameter of 200 μm from the center part of a square having a one-side length of 240 μm, was disposed to come bilaterally symmetric with respect to either one of the center line C and the diagonal line D each passing through the center 607c of the pad electrode 607. The ratio (=A/B) of area of the surface ohmic electrode 609 occupying in the total area of the open light-emitting region 607b was 28.8%.

[0049]

After forming the surface ohmic electrode 609 using ordinary vacuum evaporation and photolithography, the same

ITO film as in Example 1 was deposited as the window layer 606 by a general high-frequency spattering method. In the center of the window layer 606, a pad electrode 607 comprising gold (Au) was provided. On the back surface of the Si single crystal substrate 601, a back surface ohmic electrode 608 comprising aluminum (Al) was formed and thereafter, an LED 700 was obtained through the separation by scribing using the cleavage.

[0050]

An operating current was passed between the pad electrode 607 and the back surface ohmic electrode 608 of the LED 700, as a result, the following properties were obtained.

(a) Light emission wavelength: 440 nm

(b) Light emission luminance: 1.4 candela (cd) (provided that forward current = 20 mA)

(c) Forward voltage: 3.6 Volt (V) (provided that forward current = 20 mA)

(d) Backward voltage: 20 V or more (provided that reverse current = 10 μA)

As such, in Example 2, a group-III nitride semiconductor light-emitting diode having a low forward voltage and a high light emission intensity was obtained. Furthermore, from the near field pattern obtained for verifying the uniformity in the relative intensity of the

light emission in the open light-emitting region, it was recognized that the light emission intensity was homogeneous almost throughout the surface of the open light-emitting region. This reveals that when the surface ohmic electrode is composed of an electrode distributed to the open light-emitting region, the device operating current can homogeneously flow almost throughout the open light-emitting region.

[0051]

(Example 3)

In Example 3, a group-III nitride semiconductor LED was fabricated using a stacked layer structure obtained by stacking gallium nitride phosphide ($GaN_{1-x}P_x$, X=0.03) which works out to an ohmic contact layer 610, on the n-type gallium nitride (GaN) layer 605 constituting the uppermost layer of the stacked layer structure described in Example 1. Fig. 9 shows a schematic sectional view of the group-III nitride semiconductor LED according to Example 3. In Fig. 9, the same constituent elements as those shown in Fig. 6 are indicated by the same reference numbers as in Fig. 6 and not described here.

[0052]

The n-type gallium nitride phosphide ($GaN_{0.97}P_{0.03}$) having a phosphorus composition ratio of 3% and constituting the ohmic contact layer 610 was grown at 980°C

by a reduced-pressure MOCVD method in a reaction system of trimethylgallium ($(CH_3)_3Ga$)/ammonia (NH_3)/phosphine (PH_3)/hydrogen (H_2). The carrier concentration of the ohmic contact layer 610 was adjusted to about 2×10^{18} cm^{-3} using disilane (Si_2H_6) as the n-type doping gas. The layer thickness of the ohmic contact layer 610 was about 0.15 μm. [0053]

In the open light-emitting region 607b on the surface of the n-type $GaN_{0.97}P_{0.03}$ ohmic contact layer 610, a surface ohmic electrode 609 comprising gold (Au) and having the same outer shape and the same bottom area as in Example 2 was formed. Thereafter, the surface ohmic electrode 609 was coated with ITO film constituting the window layer 606 in the same manner as in Example 2 and in the center part of the ITO window layer, a circular pad electrode 607 consisting of a chromium (Cr) lower layer and a gold (Au) upper layer and having a diameter of 120 μm was provided. Furthermore, almost throughout the back surface of the p-type Si single crystal substrate 601, a back surface ohmic electrode 608 comprising aluminum (Al) was provided, thereby fabricating a group-III nitride semiconductor LED. [0054]

The main properties of the group-III nitride semiconductor LED of Example 3, which was fabricated by providing surface ohmic electrode 609 in the open light-

emitting region 607 on the surface of the n-type $GaN_{0.97}P_{0.03}$ ohmic contact layer 610, are shown below.

(a) Light emission wavelength: 440 nm

(b) Light emission luminance: 1.3 candela (cd) (provided that forward current = 20 mA)

(c) Forward voltage: 3.2 Volt (V) (provided that forward current = 20 mA)

(c) Backward voltage: 20 V or more (provided that reverse current = 10 μA)

The group-III nitride semiconductor LED obtained in Example 3 failed in providing clear difference in the light emission wavelength and the reverse voltage from the group-III nitride semiconductor LED obtained in Example 2, however, since the $GaN_{0.97}P_{0.03}$ layer was used as the ohmic contact layer, an effect of exhibiting high emission intensity and at the same time, low forward voltage was provided.

[0055]

[Effects of the Invention]

According to the present invention, a device operating current can uniformly flow to the light-emitting portion and this has an effect of providing a group-III nitride semiconductor LED having high light emission intensity.

Particularly, in the present invention, when the

surface ohmic electrode is disposed on the surface of the open light-emitting region other than the projective region of the pad electrode and a specific construction is employed, for example, (1) the surface ohmic electrode is disposed at the bilaterally symmetric position with respect to the center of the pad electrode, (2) the surface ohmic electrodes are disposed at isometric positions from the center of the pad electrode or (3) the surface ohmic electrodes are disposed at equal intervals from each other, this provides an effect such that the device operating current can preferentially and uniformly flow to the open light-emitting region, the current density of the device operating current capable of flowing to the open light-emitting region can be increased and therefore, a group-III nitride semiconductor LED having high light emission intensity can be obtained.

[0056]

In the present invention, when the sum of areas of surface ohmic electrodes provided in the open light-emitting region is controlled to from 5 to 30% of the total surface area of the open light-emitting region, this provides an effect of giving a group-III nitride semiconductor LED having low forward voltage while keeping high light emission intensity.

In the present invention, when the surface ohmic

electrode is provided on the surface of a gallium nitride phosphide ($GaN_{1-x}P_x$, where $0<X<1$) crystal layer, a group-III nitride semiconductor LED more reduced in the forward voltage can be provided.

[0057]

The present invention also provides an electrode for a group-III nitride semiconductor light-emitting diode, which can be used for the above-described group-III nitride semiconductor light-emitting diode.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[Fig. 1]

Fig. 1 is a schematic sectional view of a conventional group-III nitride semiconductor LED.

[Fig. 2]

Fig. 2 is a schematic plan view of a conventional group-III nitride semiconductor LED.

[Fig. 3]

Fig. 3 is a schematic sectional view of a group-III nitride semiconductor LED having a surface ohmic electrode according to the present invention.

[Fig. 4]

Fig. 4 is a schematic plan view of a group-III nitride semiconductor LED having a surface ohmic electrode according to the present invention.

[Fig. 5]

Fig. 5 is a schematic plan view of another group-III nitride semiconductor LED having a surface ohmic electrode according to the present invention.

[Fig. 6]

Fig. 6 is a schematic plan view of a group-III nitride semiconductor LED according to Example 1 of the present invention.

[Fig. 7]

Fig. 7 is a schematic sectional view cut along the broken line A-A' of the LED shown in Fig. 6.

[Fig. 8]

Fig. 8 is a schematic plan view of a group-III nitride semiconductor LED according to Example 2 of the present invention.

[Fig. 9]

Fig. 9 is a schematic sectional view of a group-III nitride semiconductor LED according to Example 3 of the present invention.

[Description of Reference Numerals]

10 light-emitting portion

100 group-III nitride semiconductor LED

101 sapphire substrate

102 buffer layer

103 lower clad layer

104 light-emitting layer

105 upper clad layer

106 p-type ohmic electrode

107 n-type ohmic electrode

200 group-III nitride semiconductor LED

201 surface ohmic electrode

202 one constituent layer of stacked layer structure

30 light-emitting portion

31 stacked layer structure

300 group-III nitride semiconductor LED

301 substrate

302 buffer layer

303 lower clad layer

304 light-emitting layer

305 upper clad layer

306 window layer

307 pad electrode

307a projective region of pad electrode

307b open light-emitting region

308 surface ohmic electrode

309 back surface ohmic electrode

507 pad electrode

507b open light-emitting region

507c center of pad electrode

508 surface ohmic electrode

509 circumference of a circle having a radius of d_1

510 circumference of circle having a radius of d_2

d_1 radius centered in the center of pad electrode

d_2 radius centered in the center of pad electrode

60 light-emitting portion

61 stacked layer structure

600 group-III nitride semiconductor LED

601 substrate

602 low temperature buffer layer

603 p-type BP single crystal layer (lower clad layer)

604 light-emitting layer

605 n-type GaN layer (upper clad layer)

606 window layer

607 pad electrode

607a projective region of pad electrode

607b open light-emitting region

607c center of pad electrode

608 back surface ohmic electrode

609 surface ohmic electrode

610 ohmic contact layer

700 group-III nitride semiconductor LED

C center line of LED passing through the center of pad electrode

D diagonal line of LED passing through the center of pad electrode

[NAME OF DOCUMENT] Abstract

[SUMMARY]

[PROBLEM TO BE SOLVED]

The solve the problem of conventional group-III nitride semiconductor LED, that is, since the LED operating current is supplied only from a pad electrode serving also as an ohmic electrode, the operating current cannot be diffused over a wide range of the light-emitting region and a group-III nitride semiconductor LED having high light emission intensity cannot be successfully provided.

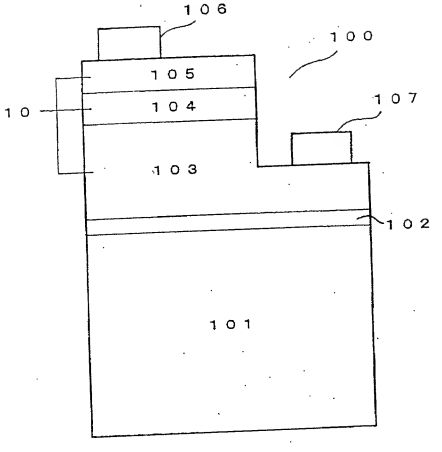
[MEANS TO SOLVE THE PROBLEM]

A group-III nitride semiconductor LED having high emission intensity is provided, which is fabricated using a stacked layer structure obtained by providing a surface ohmic electrode, a window layer composed of a conductive transparent oxide crystal layer, and a pad electrode on a conductive substrate through a boron phosphide (BP) buffer layer so as to allow the operating current to diffuse over a wide range of the light-emitting region.

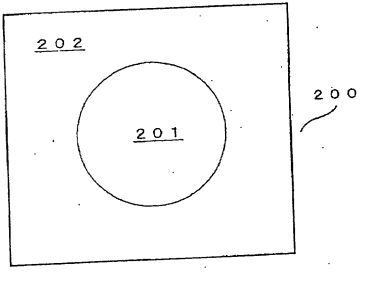
[SELECTED DRAWING] Fig. 3

[Name of Document] Drawing

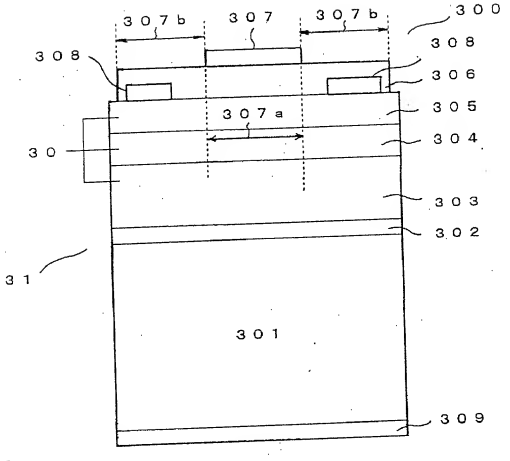
[Fig. 1]



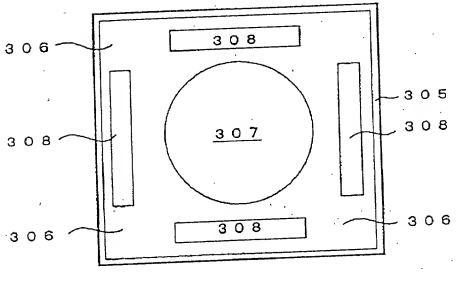
[Fig. 2]



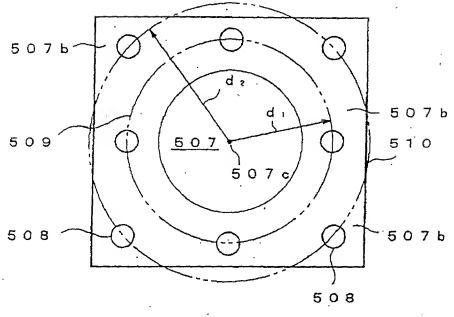
[Fig. 3]



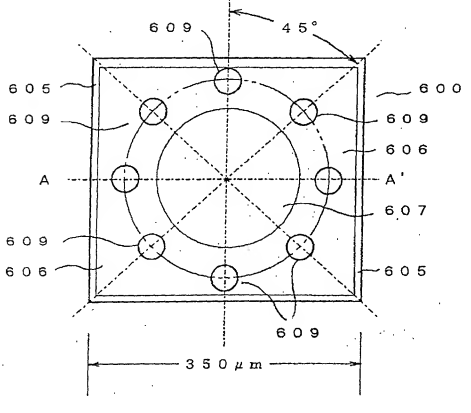
[Fig. 4]



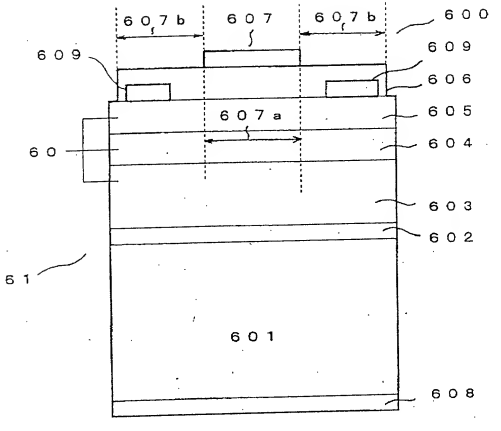
[Fig. 5]



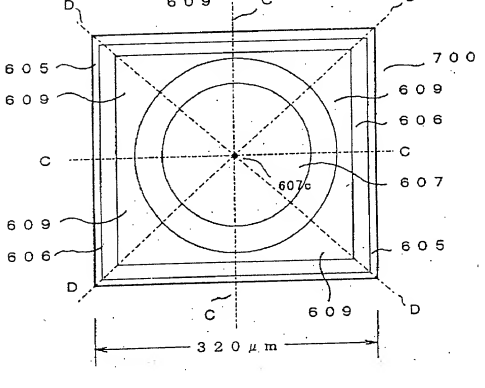
[Fig. 6]



[Fig. 7]



[Fig. 8]



[Fig. 9]